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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/519,867	MA, FAN YUNG	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1,2 and 4-7* is/are rejected.

7)☒ Claim(s) *3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of Changes

1. Claims 1, and 4-6 are newly rejected see rejections below.

Due the newly discovered reference to Zhou et al. (USPN 6,683,481) and to present new arguments to the previous rejections of claims 1-2, and 4-7 as being unpatentable over Yoshimura (USPN 5,629,642) in view of Woods (USPN 6,259,285), the finality of the previous Office action is hereby withdrawn. Applicant's submission after final filed on 21 July 2006 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, and 4-6 rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (USPN 6,683,481).

With respect to claim 1 Zhou et al. discloses in Fig. 5, a detection circuit for monitoring a supply voltages the circuit comprising:

"a comparator (501) for generating a shortfall signal (BG-POR) indicative of a shortfall of the supply voltage in relation to a reference voltage (When DD (voltage based on supply voltage) falls lower than Vref BG-POR will start to fall low. Thus when BG-POR begins to fall and reaches a low value BG-POR is output as a shortfall signal), and

an integrator (RL CL) for time-integrating the shortfall signal to form an integrated signal (due to the dual inverters of 504 and 505 RL and CL essentially integrate the BG-PORB signal. RL and CL integrate the shortfall signal by providing a delay in the falling of BG-POR, thus when BG-POR is falling RL and CL provide a delay in falling signal. This delay time of the falling signal corresponds to the time-integrating of the shortfall signal.)

wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (it can be seen that the output of the integrator is supplied as a power-on reset signal at the output of inverter 507. "for resetting a microprocessor" is merely function language that is provided by the circuit in Fig. 5 of Zhou et al., it can be seen that PORB is a reset signal. It would be apparent to one of ordinary skill in the art that power-on reset signals are used to reset microprocessors. Thus, circuit is capable of performing the intended use of resetting a microprocessor with its PORB signal.)."

With respect to claim 4, Zhou et al. discloses , a circuit comprising:

"microprocessor circuitry (Zhou et al.'s power on reset circuit is used to reset PLD (programmable logic devices), such as RAM, EEPROM, FPGA, etc., which are components of microprocessor circuitry. Also the circuitry 610 of Fig. 6 operates as a

microprocessor in that it takes and data and processes the data to complete desired functions. Which the circuit of Fig. 5 resets the circuits of Fig 6);

a comparator (501 of Fig. 5) for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (BG-POR is a signal that is indicative of a shortfall. When DD (voltage based on supply voltage) falls lower than Vref BG-POR will start to fall low. Thus when BG-POR begins to fall and reaches a low value BG-POR is output as a shortfall signal) and

an integrator (RC and CL) for time-integrating the shortfall signal to form an integrated signal (due to the dual inverters of 504 and 505 RL and CL essentially integrate the BG-PORB signal. RL and CL integrate the shortfall signal by providing a delay in the falling of BG-POR, thus when BG-POR is falling RL and CL provide a delay in falling signal. This delay time of the falling signal corresponds to the time-integrating of the shortfall signal.), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor circuit (it can be seen if Fig. 6 that the output of RL and CL output an integrated reset signal at node FF, which the reset signal is inverted through 506 to generate POR to reset the microprocessor circuitry of Fig. 6), and

reset means (506) arranged to receive the reset signal output by the UVD circuit and according to its value to initiate a reset of the microprocessor circuit." (506 receives the output from the comparator 501 and integrator RL and CL, 506 then sets the output of RL and CL to initiate a reset of the microprocessor circuit of FIG. 6 as the POR signal).

With respect to claim 5, Zhou et al. discloses in Fig. 5, a method including:

"generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (501 outputs at the BG-POR signal that detects if DD (signal based on supply voltage VDD) is less than Vref), time-integrating the shortfall signal to form an integrated signal (RL and CL act as integrator, which integrates the output of 501), and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor (as explained above the POR signal resets a microprocessor)."

With respect to claim 6, Zhou et al. discloses, "the method of claim 5 and further comprising resetting the microprocessor with the reset signal. (as explained above the reset signal of POR of Fig. 5 is used to reset the microprocessor circuitry of Fig. 6 of Zhou et al.)"

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura (5,629,642) in view of Woods (USPN 6,259,285). Yoshimura teaches, in Fig. 1 a comparator detects a shortfall in a supply by receiving a supply voltage and a

reference voltage. The output of the comparator is input to a discriminator circuit, and a delay circuit, which is used to prevent a reset when the power supply voltage is instantaneously decreased. It is used to delay the comparators signal by a prescribed amount of time. (See Col. 1 lines 51-58). This delay circuit also outputs a signal to the discriminator. The discriminator then outputs a reset signal based on the inputs of the delay and comparator circuits. Yoshimura does not teach an integrator circuit receiving the output of the comparator. Woods teaches, in Fig. 1 a delay circuit that integrates signals input to it. Woods' delay circuit as disclosed is used in a reset circuit that detects power loss. Additionally, Woods' delay circuit is used to "filter out rapid perturbations in the power supply voltage" (see Col. 2 lines 41-43).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the specific delay circuit 130 of Woods in place of the generic delay circuit 7 of Yoshimura for the purpose of having a simply constructed delay circuit that is used to delay the voltage of comparator 4, to prevent an erroneous output of the RESET signal. One skilled in the art would have been motivated to combine Yoshimura and Woods with a reasonable expectation of success.

With respect to claim 1, the above combination of Yoshimura and Woods, discloses, a detection circuit for monitoring a supply voltages the circuit comprising:

"a comparator (4 of Fig. 1 of Yoshimura) for generating a shortfall signal indicative of a shortfall of the supply voltage (VCC is supplied to 4 through 2) in relation to a reference voltage (5 supplies a reference voltage to 4, which is used with to Vcc to detect a shortfall in the supply voltage VCC.), and an integrator for time-integrating the

shortfall signal to form an integrated signal (the modified delay circuit 7 now includes the resistor and capacitor of 130 of Fig. 1 of Woods. This resistor and capacitor arrangement integrates and delays the signal of comparator 4 being input to circuit 7), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (the integrator circuit 7 is input to discriminator circuit 10, which uses both signals form 7 and 4 to output a reset signal, the resetting of the microprocessor is deemed to be intended use, and the disclosed circuit provides the possibility of being used to reset a microprocessor.)."

With respect to claim 2, the above combination of Yoshimura and Woods discloses, a circuit according to claim 1 further including "a discriminator circuit for receiving the integrated signal (10 is a discriminator that receives the integrated signal c) and at least one further output of the comparator (it can be seen that 4 also additionally outputs a signal to circuit 10 at the node between 6 and 7), and generating a reset signal using the integrated signal and the at least one further output (10 uses both signals of the comparator and the integrated signal to output the reset signal e)."

With respect to claim 4, the above combination of Yoshimura and Woods discloses, "a microprocessor circuit (circuit being reset by not(RESET) signal, see Col. 2 lines 65 not(RESET) "signal for inactivating the memory or a control IC." Clearly a microprocessor is a control IC, in that it controls information input to it and is an integrated circuit)

a comparator (4 of Fig. 1 of Yoshimura) for generating a shortfall signal indicative of a shortfall of the supply voltage (VCC is supplied to 4 through 2) in relation to a

reference voltage (5 supplies a reference voltage to 4, which is used with to Vcc to detect a shortfall in the supply voltage VCC.), and an integrator for time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 now includes the resistor and capacitor of 130 of Fig. 1 of Woods. This resistor and capacitor arrangement integrates and delays the signal of comparator 4 being input to circuit 7), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor circuit (the integrator circuit 7 is input to discriminator circuit 10, which uses both signals form 7 and 4 to output a reset signal, the resetting of the microprocessor is deemed to be intended use, and the disclosed circuit provides the possibility of being used to reset a microprocessor.), and

reset means arranged to receive the reset signal outputted by the UVD circuit according to it value to initiate a reset of the microprocessor (Yoshimura discloses in Col. 1 lines 7-9, that the circuit can be used to monitor power supply for a voltage drop in an apparatus that needs back-up of data. It is obvious to one skilled in the art use Yoshimura's circuit to reset and detect a voltage drop in the supply voltage of a microprocessor, since they are known to be used to "back-up data". Thus it would be inherent that the microprocessor had a means to receive the reset signal, that is provided to it by Yoshimura's circuit.)."

With respect to claim 5, the above combination of Yoshimura and Woods discloses, "a method of monitoring a supply voltage including:

generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (a shortfall signal is generated by 4 detecting when the

Vcc drops below reference voltage 5); time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 time integrates the output of 4 by low pass filtering the output of 4); and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor (as explained above the it would be obvious to use reset signal e, which is generated form the output signals of 4 and 7, to reset a microprocessor)."

With respect to claim 6, the above combination of Yoshimura and Woods discloses, the method of claim 5 and further comprising resetting the microprocessor with the reset signal (as stated above it would be obvious to use the reset signal e to reset a microprocessor)."

With respect to claim 7, the above combination with Yoshimura and Woods discloses, the circuit according to claim 4, wherein the UVD circuit further includes a discriminator circuit (10) for receiving the integrated signal (output of 7 c) and at least one further output of the comparator (output of 4 between the out of 6 and then input of 7), and generating a reset signal using the integrated signal and the at least one output (it can be seen that the RESET signal e is generated by 10, by receiving the signals output by 4 and 7).

Response to Arguments

Applicant's arguments with respect to claims 1, and 4-6 with respect to Winebarger have been considered but are moot in view of the new ground(s) of rejection.

With respect to claims 1-2, and 4-7 rejected under 35 USC 103(a) as being unpatentable over Yoshimura (USPN 5,629,642) in view of Woods (USPN 6,259,285), Examiner finds Applicant's arguments unpersuasive. There is no recitation found in Yoshimura (USPN 5,629,642) that requires delay circuit 7 of Fig. 1 to be a "digital delay". In fact 7 is merely a generic delay circuit that encompasses all forms of delay. The timing diagrams of Fig. 5 of Yoshimura are for illustrative purposes only. While they do not show curved, or exponential rising and falling signals the signals still can be indicative of analog signals and are only drawn to be square (digital) signals to illustrate how the circuit operates. However, there is no recitation found anywhere in the reference of Yoshimura that requires the signals to be "digital delay" signals. Also, it would be understood by one of ordinary skill in the art that "analog delay" circuits such as that of 130 of Fig. 1 of Woods do in fact create time-shifted delays. For instance, Applicant states that analog delay circuits effect "the rate at which the output voltage rises to a peak is delayed". Thus, if the peak voltage is delayed with time, then the logic high (signal equal to 1) would be delayed with time also, because the analog delay circuit would delay the amount of time required for a logic high to be achieved. Thus this would shift, with respect to time, when the input to 9 would achieve a logic high, or conversely a logic low. Further, it would be understood that the delay times of 130 of Woods can be selected to the proper delay time by properly selecting the RC constants of 130 of Woods. Woods circuit is simply constructed, and used to rapidly filter erroneous signal levels, therefore one would be sufficiently motivated to use the specific error filtering delay circuit simply constructed delay circuit of Woods with Yoshimura

generic delay circuit 7. Further it is notoriously well-known to combine RC delays with digital logic circuits.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fig. 9 of Shimoda (USPN 6,188,266) discloses and under voltage detecting comparator, which outputs to an integrator.

Figs. 5 and 6 of Hoang (USPN 5,497,112) disclose a under voltage detecting comparator that outputs a shortfall signal (PUNDER) of a detected supply voltage signal. In Fig. 6 Hoang discloses an integrator (T76-T78), which outputs to a discriminator (N3). However, Hoang's integrator integrates the over voltage detection signal to insure that the supply voltage has returned to a normal supply range.

Allowable Subject Matter

Claims 3 and 8 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 3, there was no prior art found that taught the used of a control signal control switches of the discriminator circuit of Yoshimura. Also, there was no prior art found that provided motivation for combining Yoshimura with a switched discriminator that accepts signals output form a comparator, and an integrated signal that is generated form a different output of a comparator. Thus claim 3 is allowable, and

claim 8 is allowed based on the same reasoning as claim 3.

Claims 9 and 10 are allowed

With respect to claim 9, there is no cited art that teaches the use of a control signal control switches of the discriminator circuit of Yoshimura. Also, there is no cited art that provides motivation for combining Yoshimura with a switched discriminator that accepts signals output form a comparator, and an integrated signal that is generated form a different output of a comparator. Thus claim 9 is allowed, and claim 10 is allowed based on the same reasoning as claim 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
August 1, 2006

LINH MY NGUYEN
PRIMARY EXAMINER